A 16 GHz GaAs FET Frequency Divider

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Abstract

A GaAs FET regenerative frequency divider operating at K_u-band is described, employing a 0.5 μm gate length device biased in the vicinity of pinch-off so as to provide both the gain and the nonlinear properties required for achieving frequency division. The study includes measured circuit responses as functions of drive level for single-tone CW, single-tone pulsed, and two-tone CW excitations.

Introduction

Microwave frequency divider circuits can provide attractive system alternatives in areas such as communication links, phase-locked loops, and electronic warfare. Various frequency divider concepts have been reported in the literature, with each concept belonging to either one of two basic categories. The first category comprises circuits which operate like digital frequency counters. Besides available high-speed logic implementations for lower microwave frequencies, this category also includes those divider circuits that employ two-terminal or three-terminal transferred-electron devices.[1] The second category contains the regenerative circuits which operate on the principle of induced subharmonic oscillation.[2,3,4] Varactor frequency dividers[5] also belong in this category, as they constitute an implicit realization of the regenerative principle. The subject of the present paper is to study feasibility and performance characteristics of a regenerative frequency divider at K_u-band which employs a single-gate GaAs FET.

The GaAs FET Frequency Divider Circuit

The regenerative frequency divider concept in its discrete component implementation, as indicated in Fig. 1, involves a mixer element and an amplifying subharmonic feedback loop. The circuit studied here uses a GaAs FET in grounded source configuration to simultaneously perform the mixing and the amplifying tasks. For this purpose, the transistor is biased class AB in order to achieve mixing through transconductance modulation in the vicinity of pinch-off, while maintaining sufficient gain at the subharmonic frequency. The transistor is embedded in a composite coupling network that provides input and output matching, and furnishes appropriate feedback for sustaining subharmonic oscillation.

The circuit is designed to accommodate a 16 GHz input signal and is implemented in microstrip on a 0.25 mm thick fiberglass reinforced teflon substrate as depicted in Fig. 2. The transistor used in this experiment is one cell of an Avantek M110 GaAs FET with a gate length of 0.5 μm, a gate width of 375 μm, and a pinch-off voltage of -2.9 V. The drain-source and gate-source bias voltages are $V_{DS} = +3.0$ V and $V_{GS} = -2.6$ V, respectively. Subharmonic feedback at 8 GHz is primarily controlled by a miniature 5 nH air coil inductor and a 5 pF silicon nitride blocking capacitor connected in series between drain and gate terminals. The inductor consists of seven turns of gold wire with a coil diameter of 300 μm. The input network provides conjugate couplex matching to the gate port of the device at 16 GHz, while blocking the generated 8 GHz subharmonic signal. Likewise, the output network matches the drain port of the device to a 50 ohm load at 8 GHz and rejects the 16 GHz signal component.

Feedback determines the turn-on threshold which the incident RF power must exceed before regenerative frequency division sets in. Unlike varactor frequency dividers where the minimum achievable threshold is determined by varactor losses, the FET divider permits the threshold to be reduced to arbitrarily low levels. There is, however, a practical lower bound on the threshold level which is dictated by the necessity to safeguard against spurious oscillations. In the present case, feedback and input-output matching conditions were derived by first designing the circuit to be on the verge of oscillation at the subharmonic frequency of 8 GHz, employing existing techniques,[6] and then reducing the amplitude of the feedback signal by 3 dB to achieve a conservative safety margin.

Performance of the GaAs Frequency Divider

Characteristic of a regenerative frequency divider is the time-delay the leading edge of an RF pulse experiences in the division process as the subharmonic oscillation builds up. This is demonstrated for the GaAs FET divider circuit by applying a pulsed 16 GHz test signal of 200 ns pulse duration to its input and then observing the pulsed 8 GHz response on a sampling scope. Figure 3 shows the shape of the incident 16 GHz pulse. Using the same time scale, Fig. 4 depicts the frequency-divided output signal. It is apparent how the leading edge delay decreases as the output signal responds to increasing 16 GHz drive levels.

As for the single-tone CW performance of the divider, Fig. 5 shows RF conversion gain as a function of 16 GHz input drive level. The turn-on threshold occurs at around 6.5 dBm of incident power and is primarily a function of the amount of feedback introduced external to the transistor. Also shown in Fig. 5 is

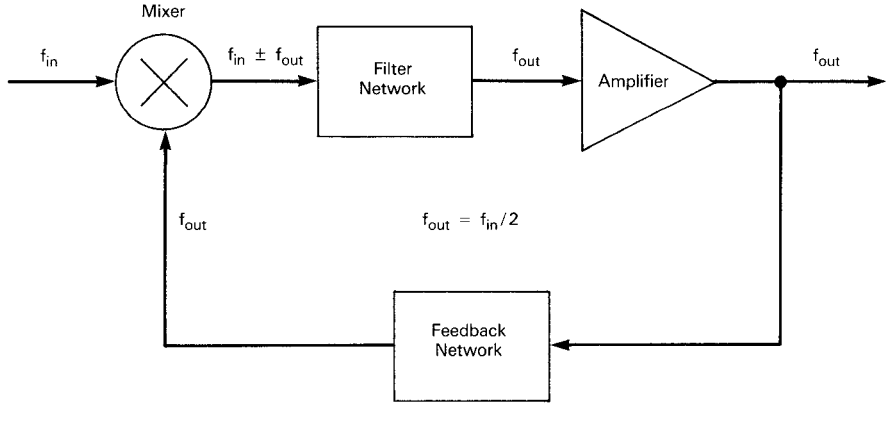

Fig. 1 — General concept of regenerative frequency division

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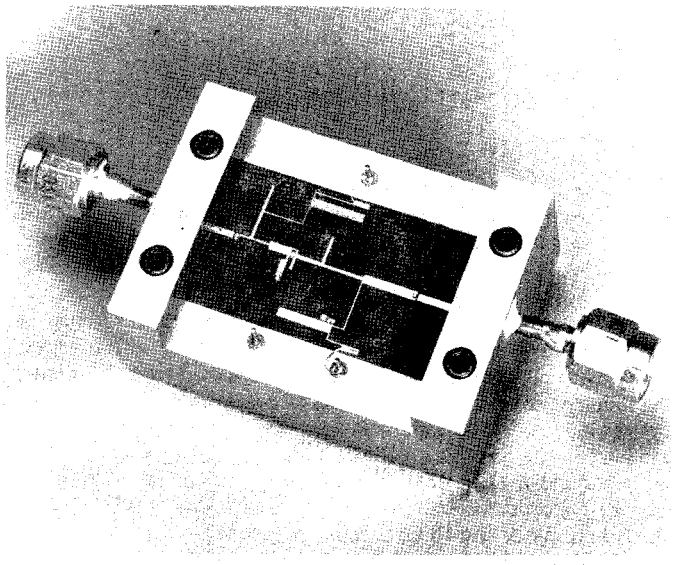

Fig. 2 — Experimental 16 GHz GaAs FET frequency divider, implemented in microstrip on a 0.25 mm thick fiber-glass reinforced teflon substrate, using a transistor with a 0.5 μm by 375 μm gate geometry

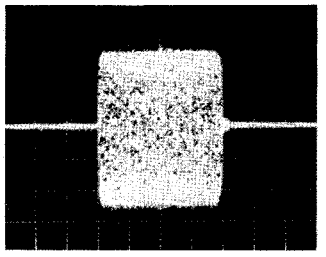

Fig. 3 — Incident 16 GHz pulse of 200 ns duration. Time scale: 50 ns per division.

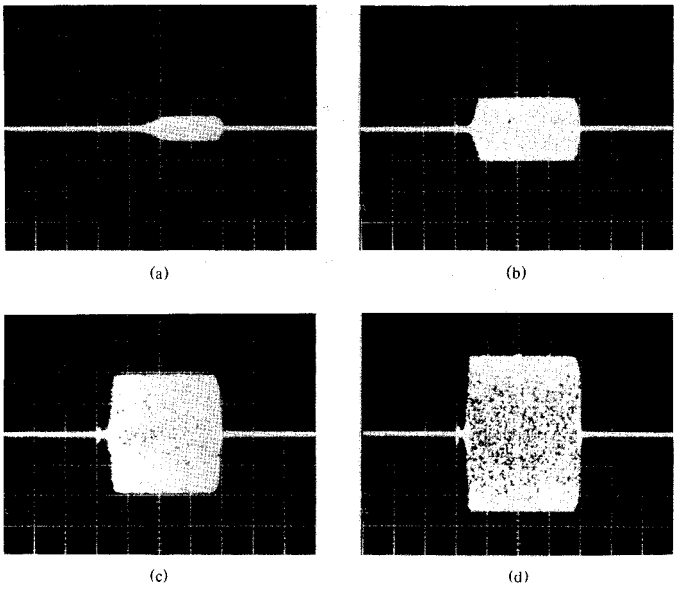

Fig. 4 — 8 GHz pulsed output response of the GaAs FET frequency divider for 16 GHz input peak power levels of: (a) +7 dBm, (b) +10 dBm, (c) +13 dBm, and (d) +16 dBm. Time scale: 50 ns per division.

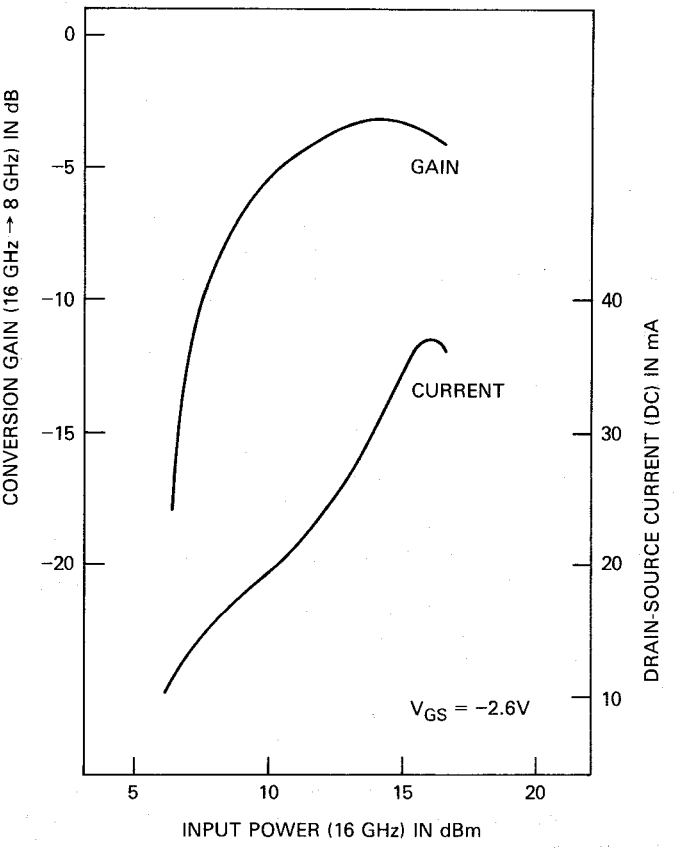

Fig. 5 — Single-tone characteristics of the GaAs FET frequency divider for bias voltages $V_{GS} = -2.6$ V and $V_{DS} = +3.0$ V

the DC drain-source current of the transistor which increases with drive level due to the rectifying action associated with operation in the vicinity of pinch-off. Relative to the input signal, the test circuit exhibits a conversion gain 3 dB bandwidth of approximately 0.6 GHz for the stated nominal bias conditions. Although main emphasis has been focused on studying principal characteristics of GaAs FET divider operation without specific concern for bandwidth, appreciably wider bandwidths can be readily obtained in exchange for increased circuit complexity. This could include the use of a balanced circuit configuration to achieve separation of input and output signals through symmetry, thus bypassing some of the bandwidth limitations associated with the use of conventional filtering. In this context, it is also interesting to note that—over the entire frequency range of operation—the GaAs FET divider circuit did not exhibit any signs of hysteresis effects versus drive level such as encountered in varactor dividers.[5] However, this does not necessarily indicate that hysteresis effects cannot occur in GaAs FET divider circuits.

Ideally, a frequency divider would translate a given input spectrum to the subharmonic frequency band by frequency dividing each spectral component in a similar fashion. In special cases this may be readily achieved—such as when dealing with a class of FM input signals.[3,4] But in general, however, the regenerative divider circuit is apt to pick the dominant component of the input spectrum and only subject it to frequency division, while letting the frequency-divided principal component then act, in effect, as a down-converting local oscillator relative to the rest of the spectrum. Depending on the type of spectrum involved, this can lead to confusion in interpreting the output signal. In addressing this aspect, the FET divider response to various two-tone CW input signals has been studied. A sample of the findings is portrayed in the sequence of spectrum analyzer oscillograms shown in Fig. 6.

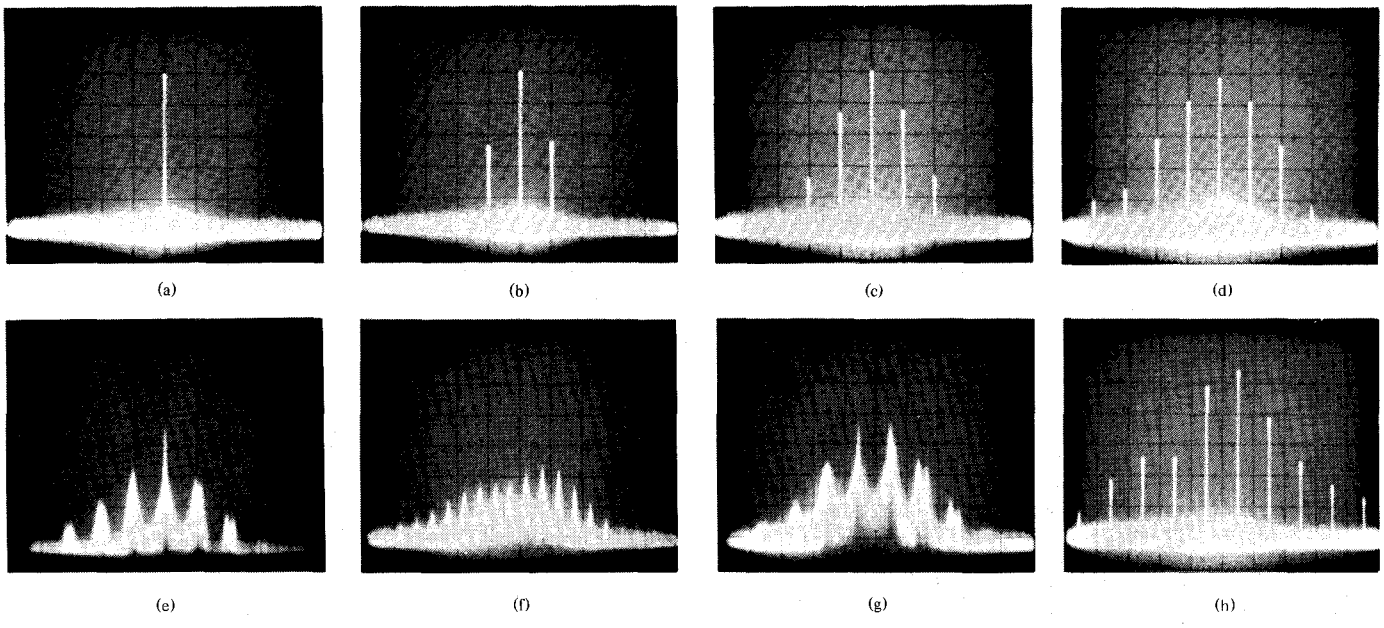

Fig. 6 — Output spectra for two-tone excitations consisting of a fixed +10 dBm signal at 16 GHz and second signal at 16.1 GHz whose amplitude varies according to: (a) 0 mW, (b) −10 dBm, (c) 0 dBm, (d) +7 dBm, (e) +9 dBm, (f) +10 dBm, (g) +11 dBm, and (h) +13 dBm. Frequency scale: 0.1 GHz per division centered at 8.0 GHz.

The input signal is composed of a fixed +10.0 dBm CW component at 16.0 GHz, and a variable-amplitude CW component at 16.1 GHz covering the range from zero to 20 mW (13 dBm). As the amplitudes of the two signals approach one another and the 16.1 GHz signal begins to challenge the dominance of the 16.0 GHz signal, the output response becomes poorly defined and very noisy (Figs. 6e through 6g). Thereafter, the 16.1 GHz signal and its frequency-divided counterpart take over the lead (Fig. 6h).

Conclusions

As illustrated by the test circuit under investigation, GaAs FETs provide an attractive, conceptually simple means for achieving regenerative frequency division in the microwave range. Practical application of any type of regenerative frequency divider is inherently constrained by its threshold characteristics, saturation effects, pulse leading edge delay, and limitations related to multiple input signals overlapping in the time domain. GaAs FET frequency dividers naturally remain subject to the same kinds of limitations. But within these constraints, as demonstrated in this study, the GaAs FET divider offers an alternative exhibiting well behaved performance characteristics and, above all, reflecting the easy designability common to GaAs FET circuits in general.

References

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